OIPE JC17
JUL 0 8 2004
PATENT & TRADEMARK OFFICE

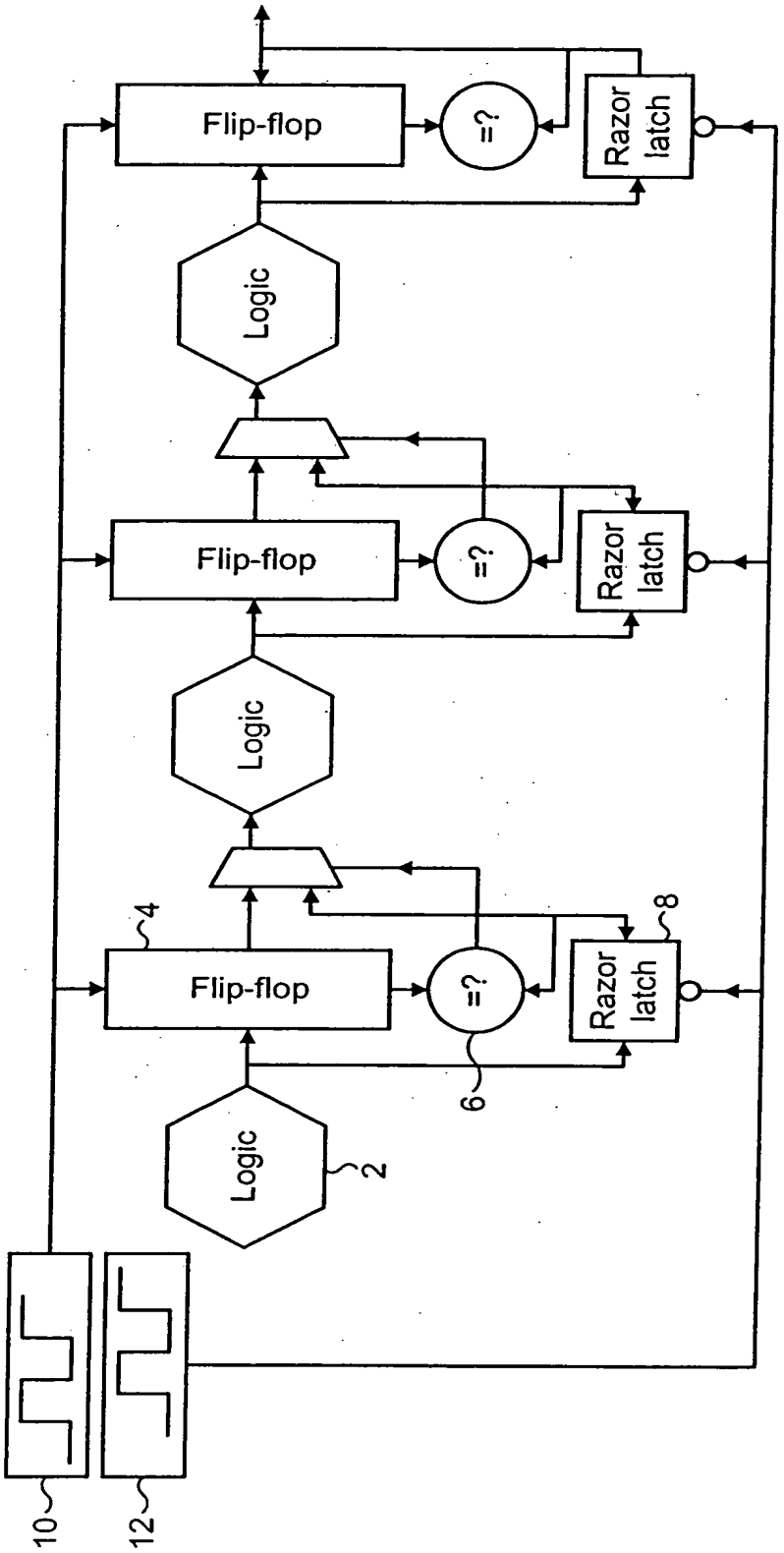


FIG. 1

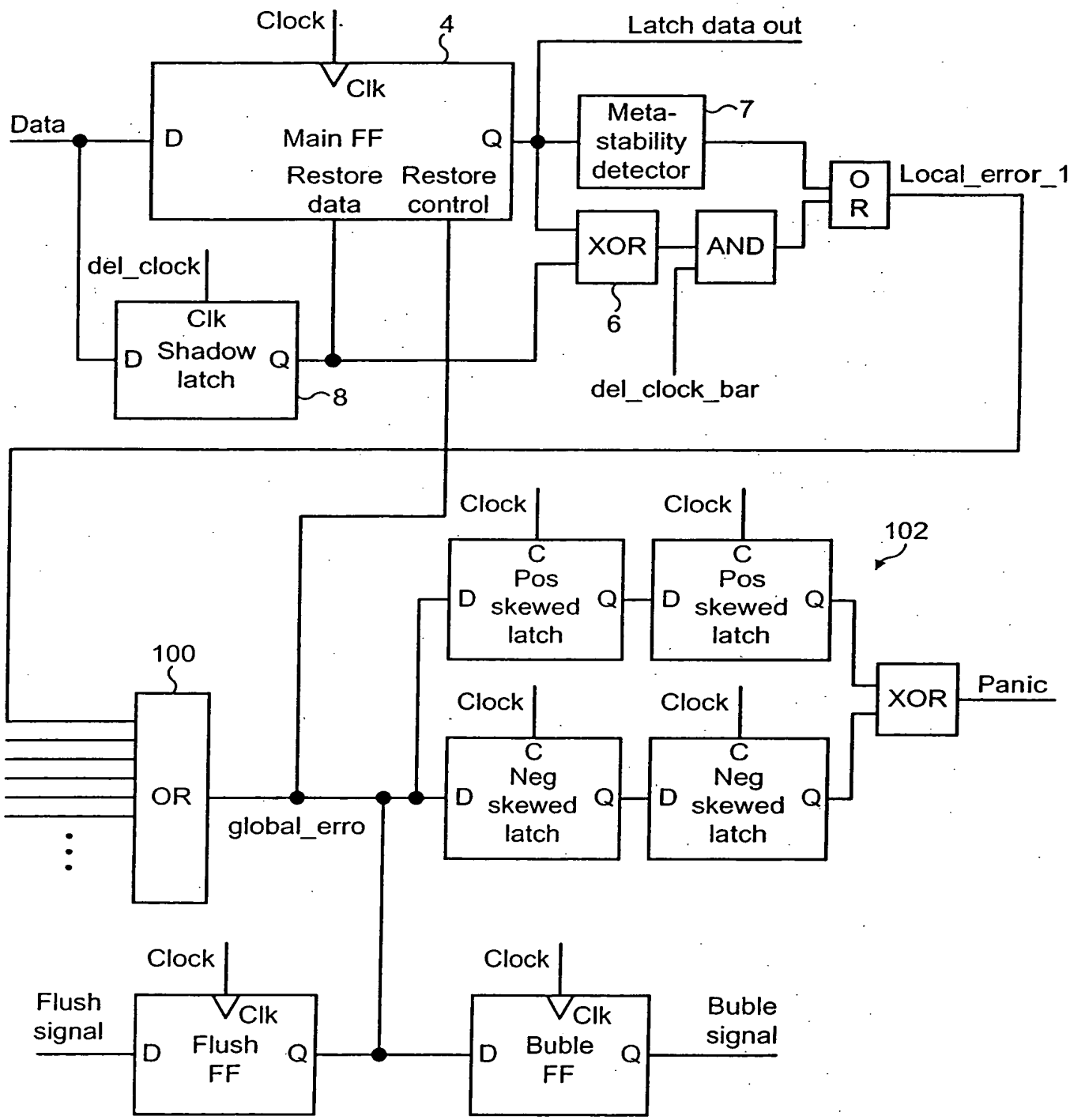

Clock
4
Clk
Data
D
Main FF
Q
Restore data
Restore control
Latch data out
Meta-stability detector
7
O R
Local_error_1
XOR
AND
6
del_clock
Clk
D
Shadow latch
Q
8
del_clock_bar
Clock
Clock
102
C
Pos skewed latch
D
Q
100
XOR
Panic
Clock
Clock
C
Neg skewed latch
OR
global_erro
Clock
Clock
Flush signal
Clk
Flush FF
Buble signal
Buble FF

FIG. 2

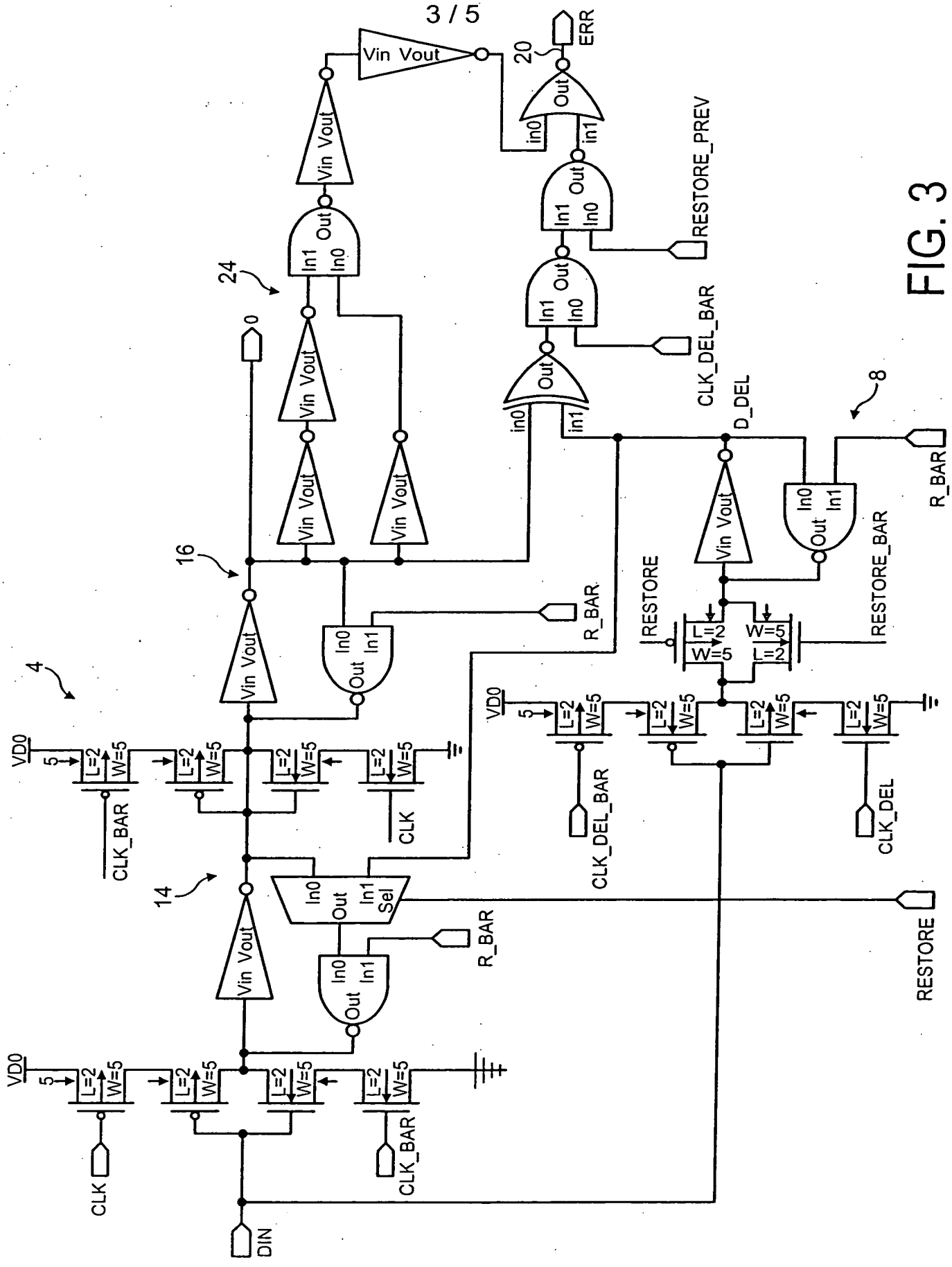

Vin Vout
ERR
20
Out
in0
in1
RESTORE_PREV
In1 Out In0
CLK_DEL_BAR
D_DEL
24
0
8
R_BAR
16
RESTORE
RESTORE_BAR
In0 In1 Out
4
VD0
5
L=2
W=5
CLK_BAR
CLK
CLK_DEL
14
In0 In1 Out Sel
DIN

FIG. 3

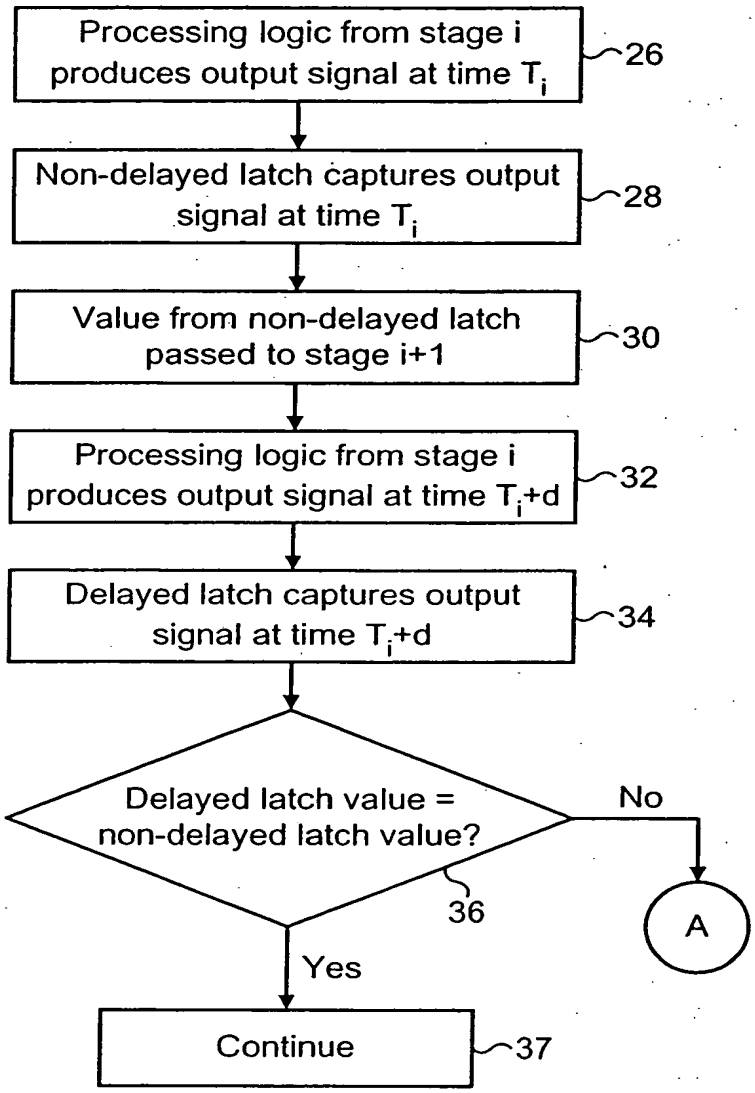

Processing logic from stage i produces output signal at time T_i
26
Non-delayed latch captures output signal at time T_i
28
Value from non-delayed latch passed to stage i+1
30
Processing logic from stage i produces output signal at time T_i+d
32
Delayed latch captures output signal at time T_i+d
34
Delayed latch value = non-delayed latch value?
36
No
A
Yes
Continue
37

FIG. 4A

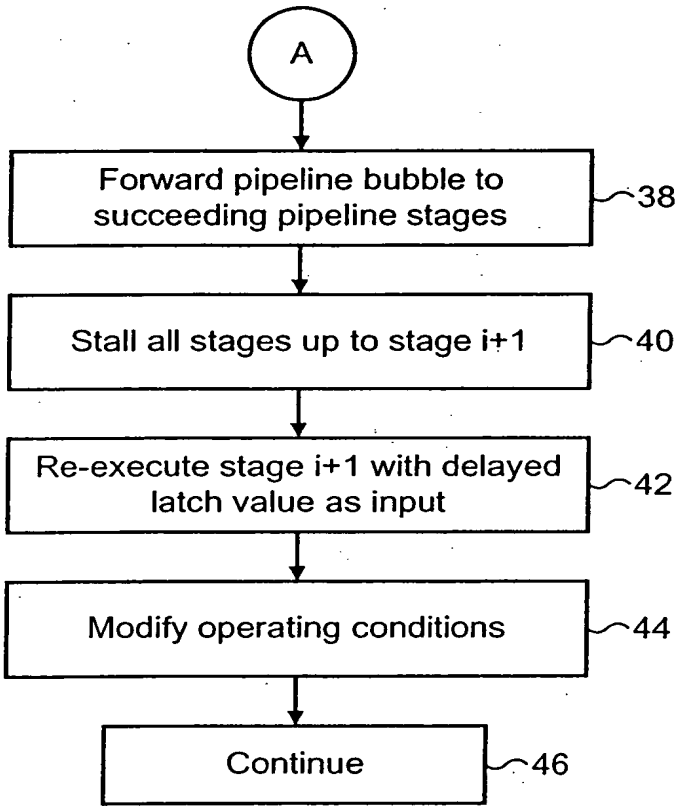

A
Forward pipeline bubble to succeeding pipeline stages
38
Stall all stages up to stage i+1
40
Re-execute stage i+1 with delayed latch value as input
42
Modify operating conditions
44
Continue
46

FIG. 4B

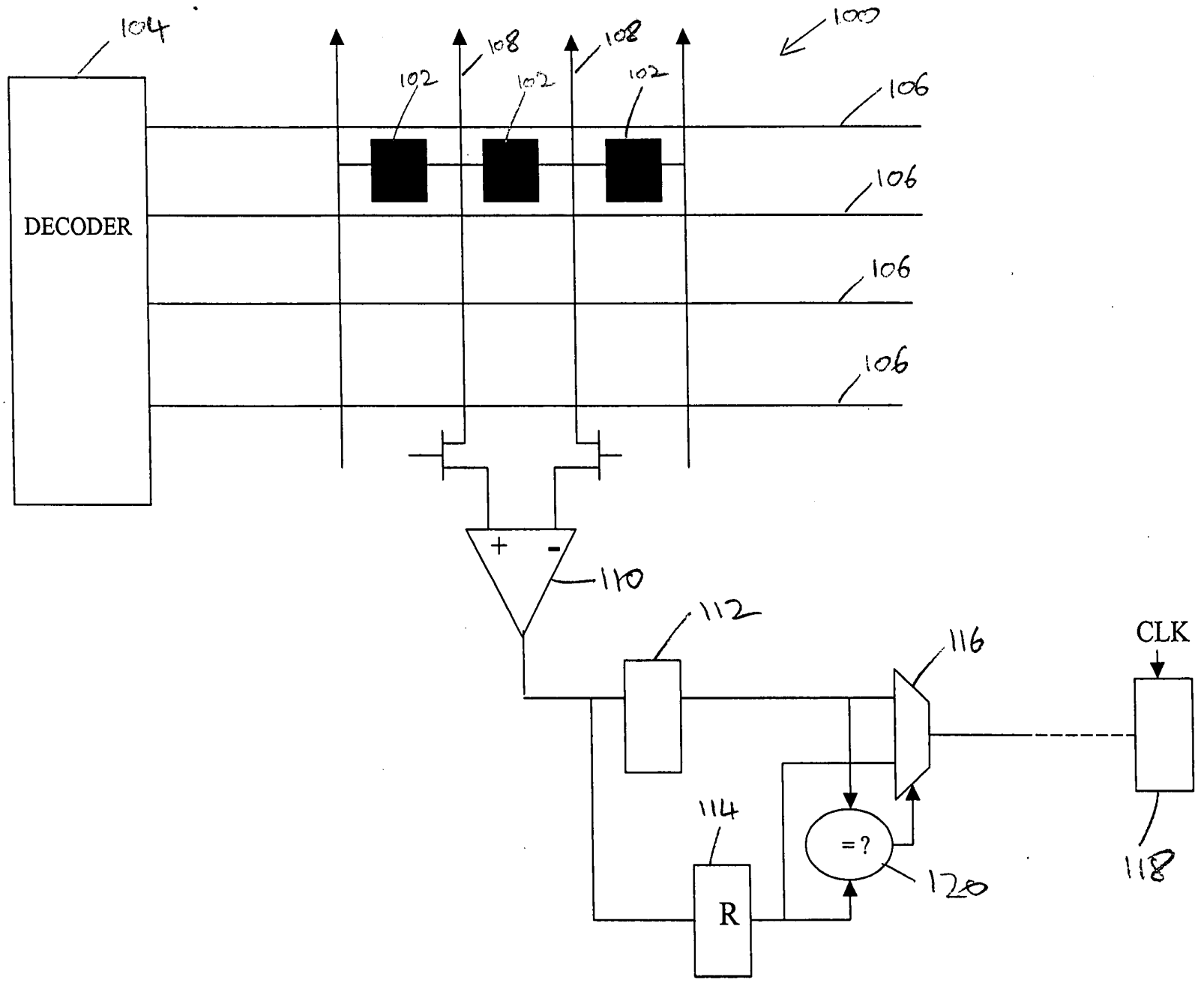

104
100
108
108
102
102
102
106
106
106
106
DECODER
+
-
110
112
116
CLK
114
=?
120
118
R

Fig 5

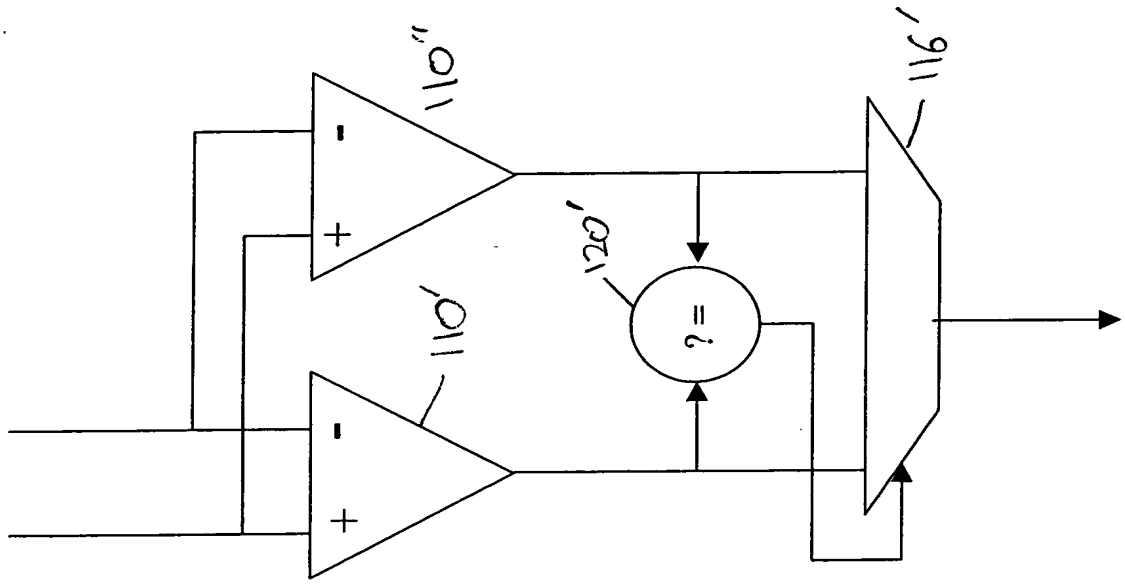


Fig 6

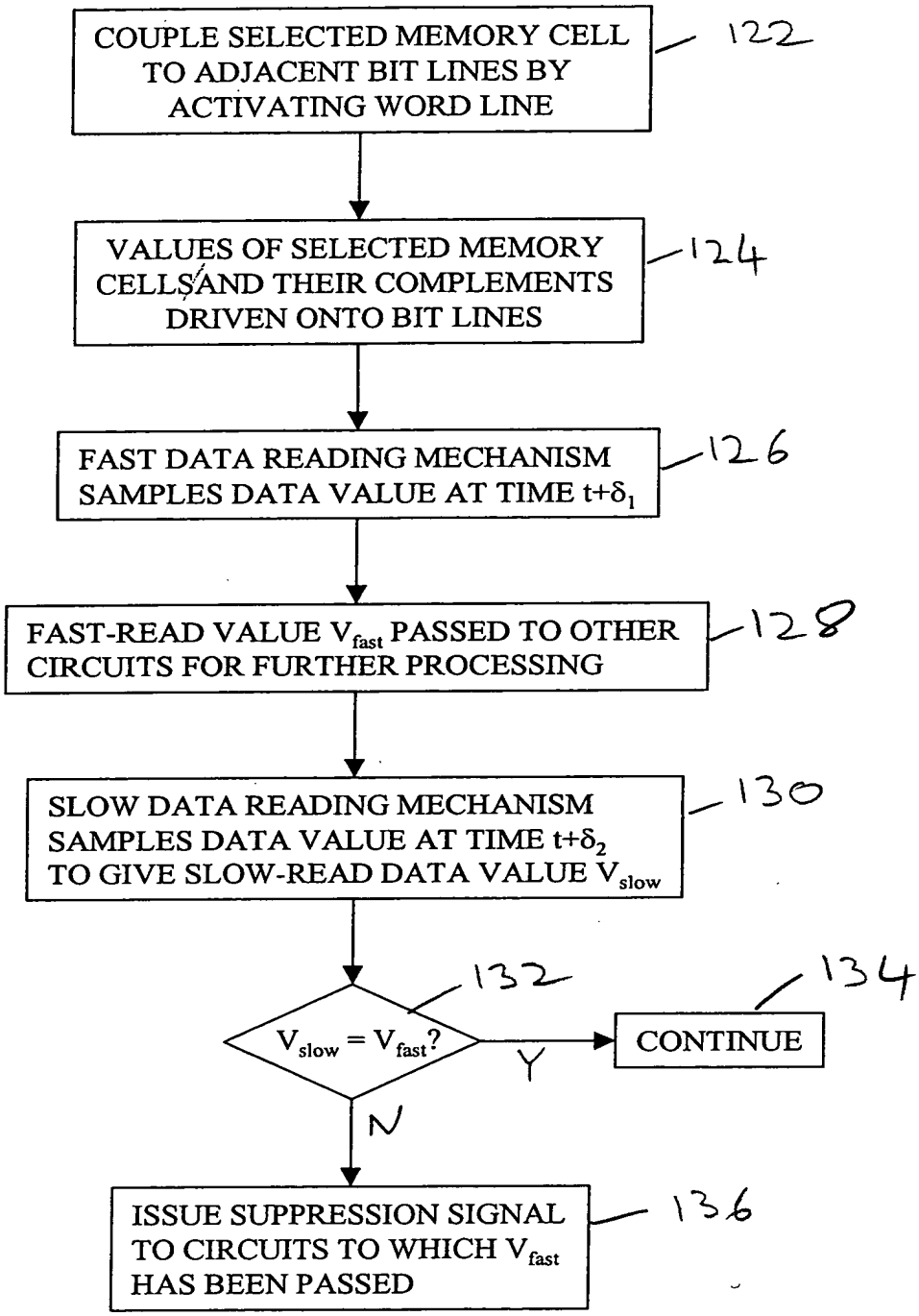

COUPLE SELECTED MEMORY CELL TO ADJACENT BIT LINES BY ACTIVATING WORD LINE
122
VALUES OF SELECTED MEMORY CELLS AND THEIR COMPLEMENTS DRIVEN ONTO BIT LINES
124
FAST DATA READING MECHANISM SAMPLES DATA VALUE AT TIME $t+\delta_1$
126
FAST-READ VALUE V_{fast} PASSED TO OTHER CIRCUITS FOR FURTHER PROCESSING
128
SLOW DATA READING MECHANISM SAMPLES DATA VALUE AT TIME $t+\delta_2$ TO GIVE SLOW-READ DATA VALUE V_{slow}
130
$V_{slow} = V_{fast}$?
132
Y
CONTINUE
134
N
ISSUE SUPPRESSION SIGNAL TO CIRCUITS TO WHICH V_{fast} HAS BEEN PASSED
136

Fig 7

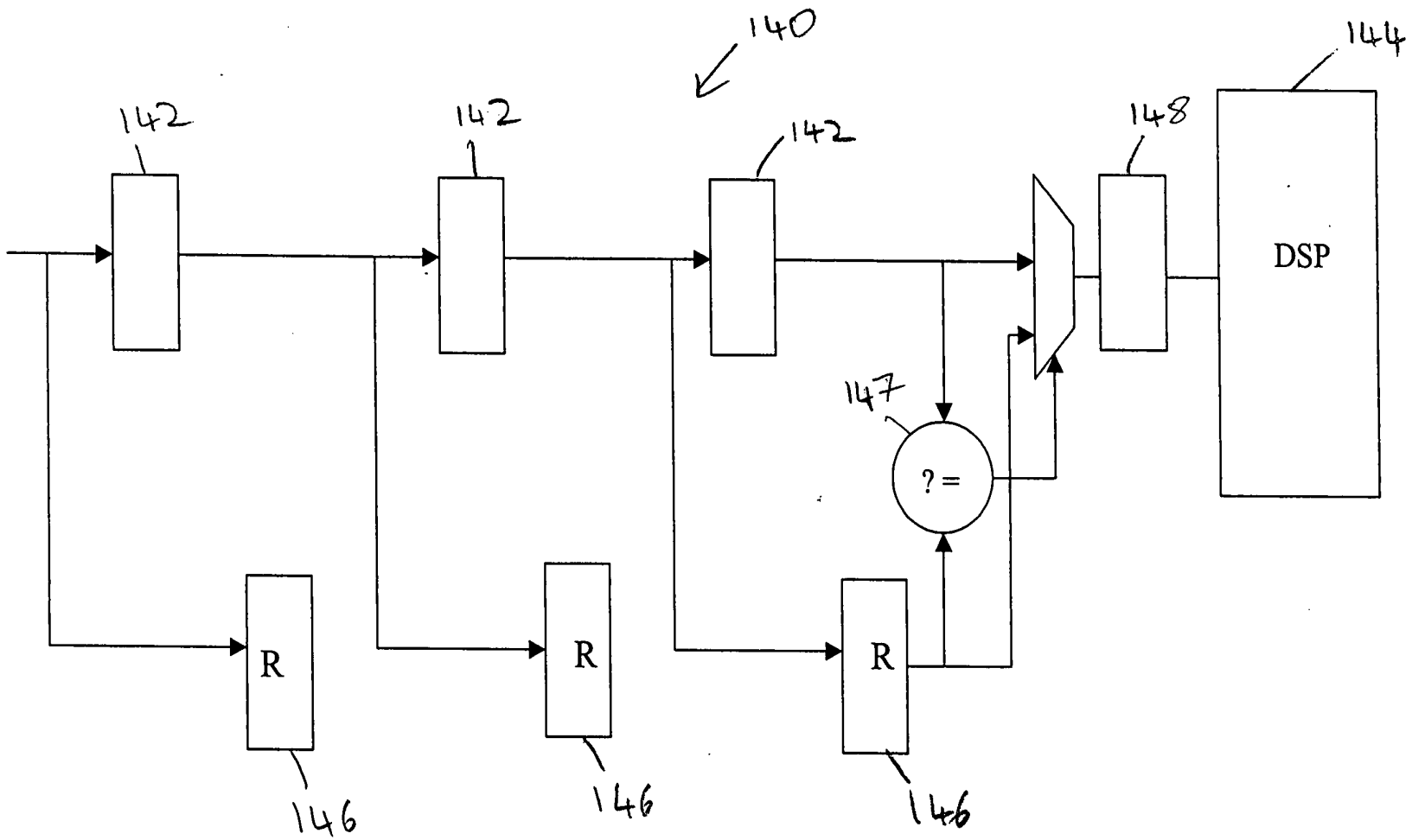


Fig 8

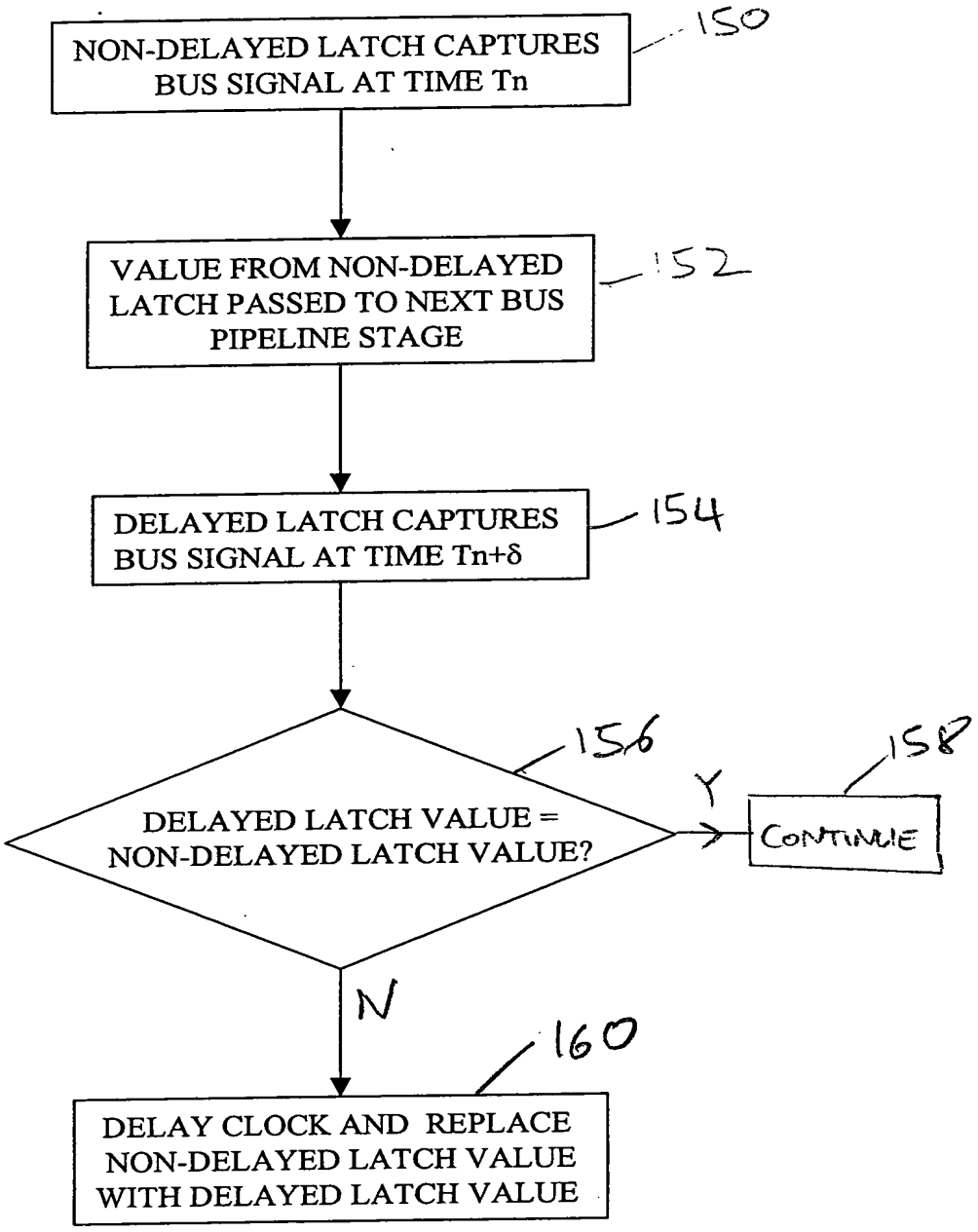

NON-DELAYED LATCH CAPTURES BUS SIGNAL AT TIME Tn
150
VALUE FROM NON-DELAYED LATCH PASSED TO NEXT BUS PIPELINE STAGE
152
DELAYED LATCH CAPTURES BUS SIGNAL AT TIME Tn+δ
154
DELAYED LATCH VALUE = NON-DELAYED LATCH VALUE?
156
Y
CONTINUE
158
N
DELAY CLOCK AND REPLACE NON-DELAYED LATCH VALUE WITH DELAYED LATCH VALUE
160

Fig 9

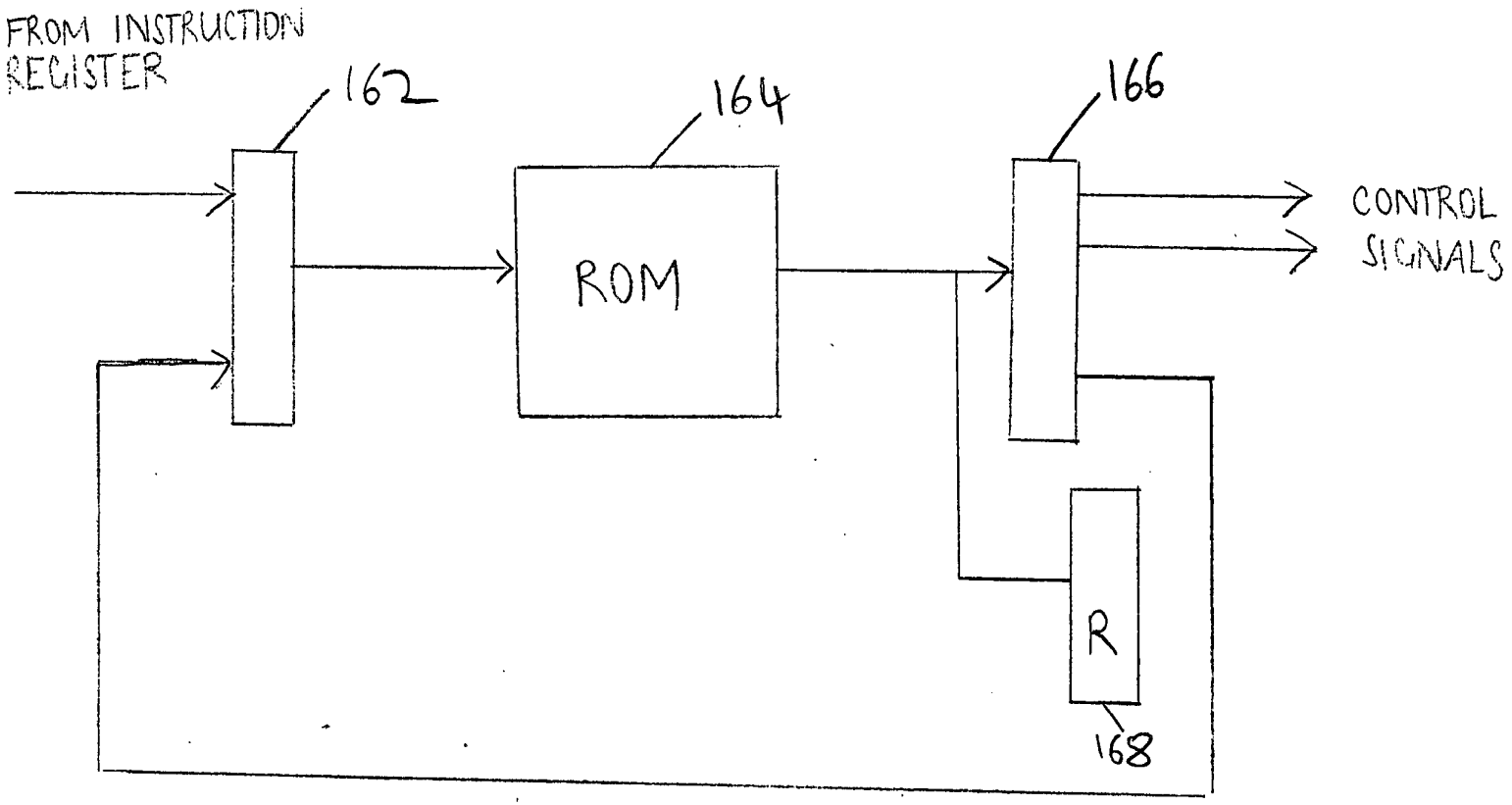

FROM INSTRUCTION REGISTER
162
164
166
ROM
CONTROL SIGNALS
R
168

Fig 10

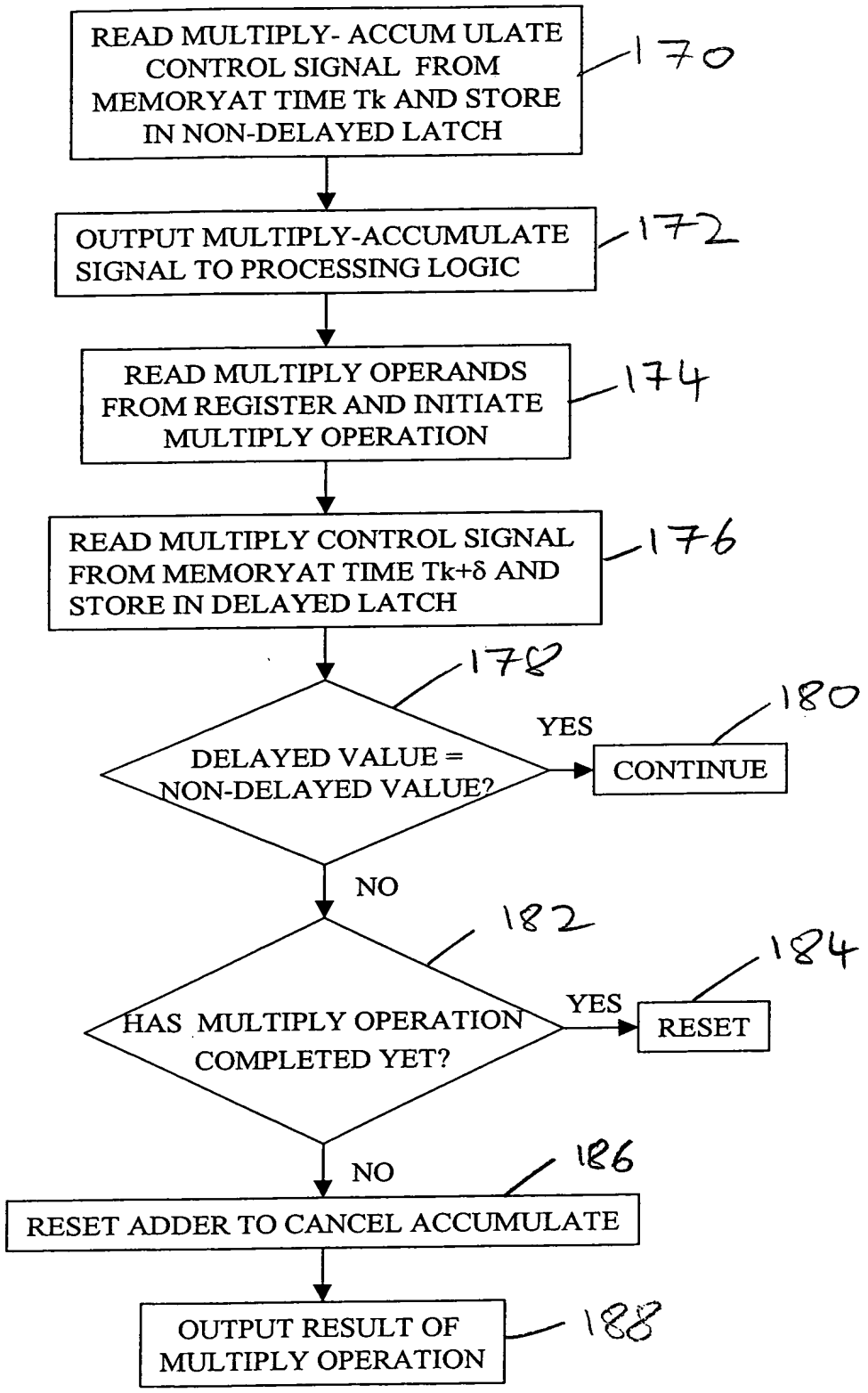

READ MULTIPLY- ACCUM ULATE CONTROL SIGNAL FROM MEMORYAT TIME Tk AND STORE IN NON-DELAYED LATCH
170
OUTPUT MULTIPLY-ACCUMULATE SIGNAL TO PROCESSING LOGIC
172
READ MULTIPLY OPERANDS FROM REGISTER AND INITIATE MULTIPLY OPERATION
174
READ MULTIPLY CONTROL SIGNAL FROM MEMORYAT TIME Tk+δ AND STORE IN DELAYED LATCH
176
178
DELAYED VALUE = NON-DELAYED VALUE?
YES
180
CONTINUE
NO
182
HAS MULTIPLY OPERATION COMPLETED YET?
YES
184
RESET
NO
186
RESET ADDER TO CANCEL ACCUMULATE
OUTPUT RESULT OF MULTIPLY OPERATION
188

Fig 11

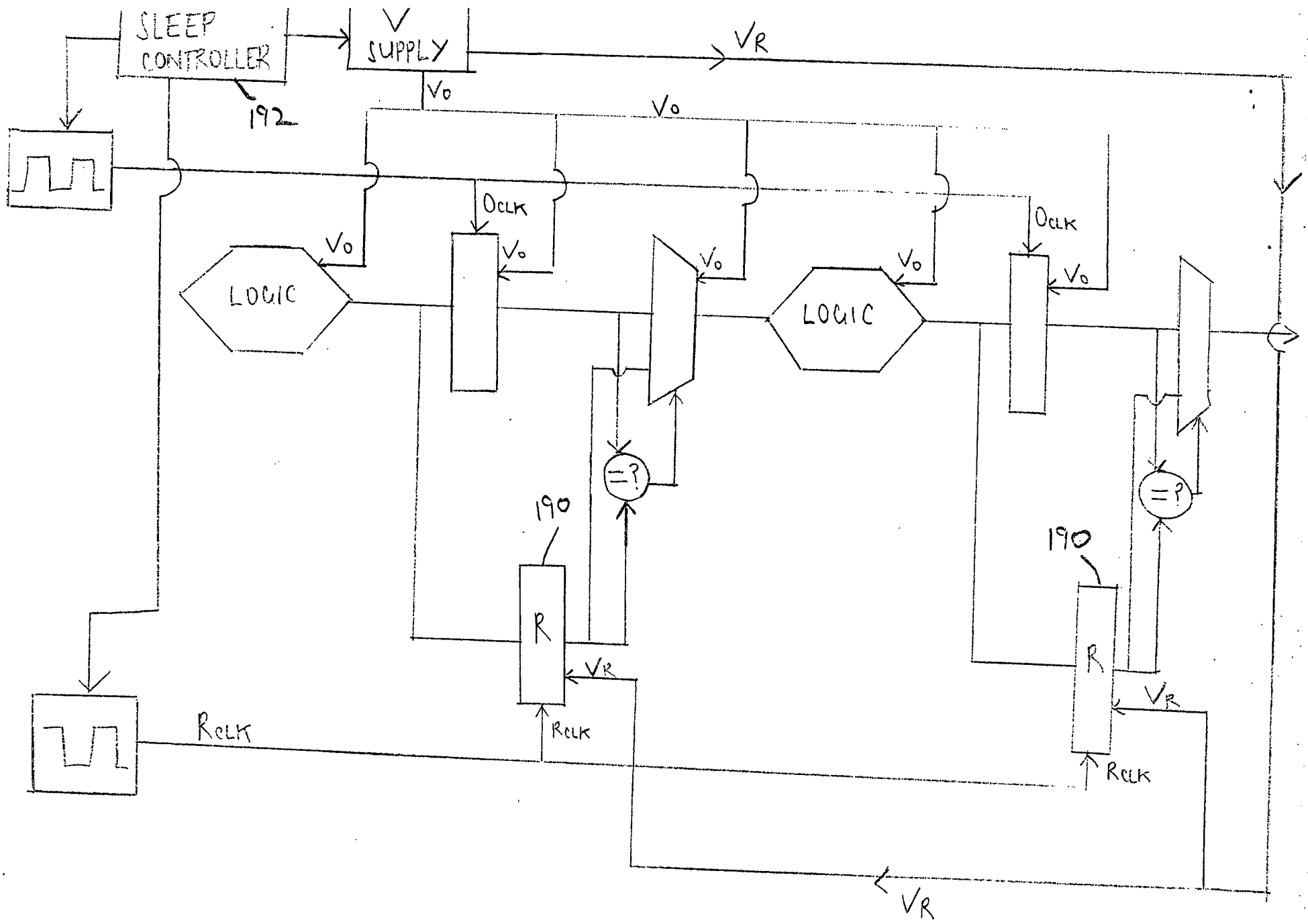

SLEEP CONTROLLER
192
V SUPPLY
VR
Vo
Vo
OCLK
Vo
LOGIC
Vo
Vo
OCLK
Vo
LOGIC
Vo
=?
=?
190
190
R
R
VR
VR
RCLK
RCLK
RCLK
VR

Fig 12

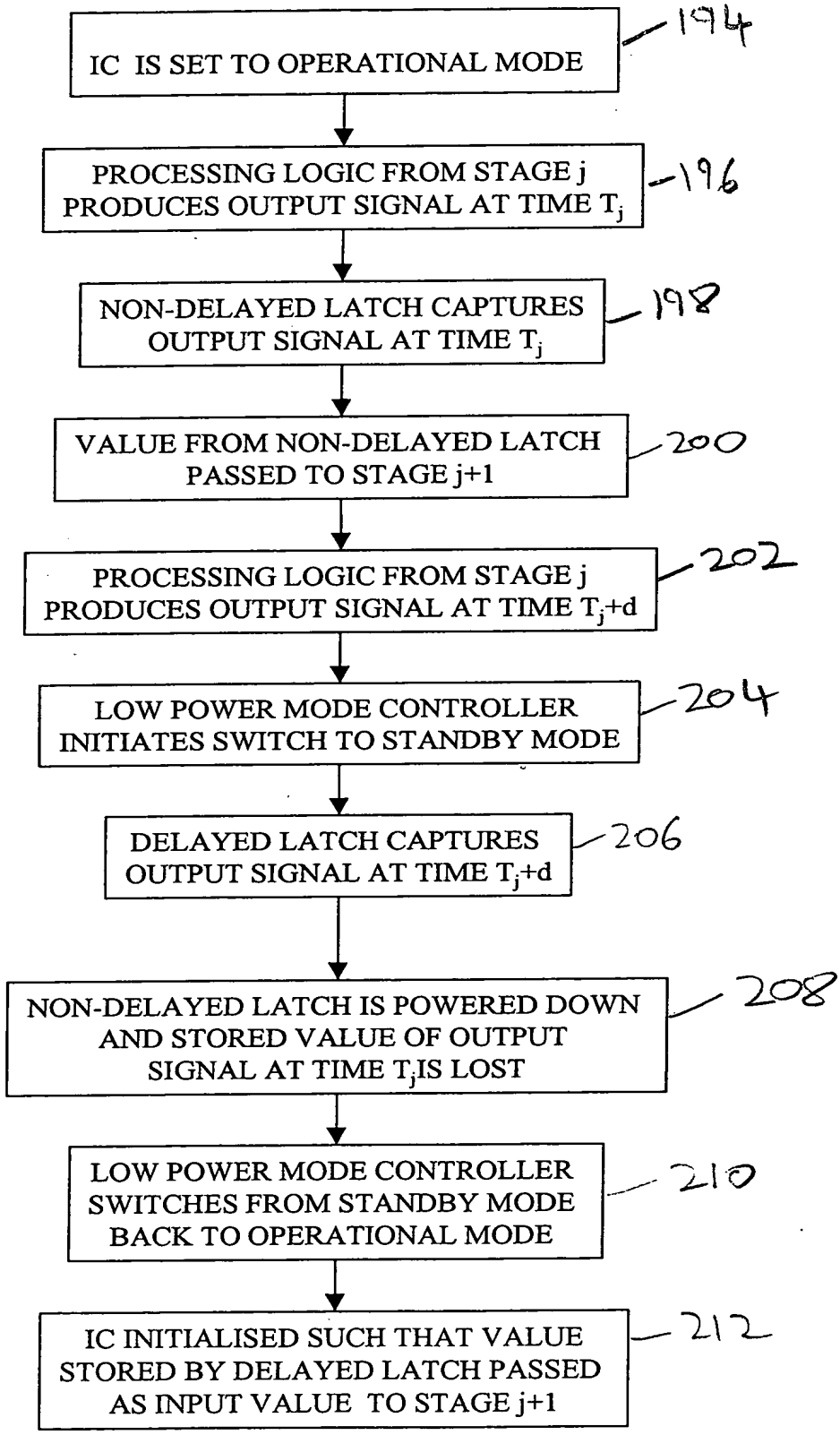

IC IS SET TO OPERATIONAL MODE
194
PROCESSING LOGIC FROM STAGE j PRODUCES OUTPUT SIGNAL AT TIME T_j
196
NON-DELAYED LATCH CAPTURES OUTPUT SIGNAL AT TIME T_j
198
VALUE FROM NON-DELAYED LATCH PASSED TO STAGE j+1
200
PROCESSING LOGIC FROM STAGE j PRODUCES OUTPUT SIGNAL AT TIME T_j+d
202
LOW POWER MODE CONTROLLER INITIATES SWITCH TO STANDBY MODE
204
DELAYED LATCH CAPTURES OUTPUT SIGNAL AT TIME T_j+d
206
NON-DELAYED LATCH IS POWERED DOWN AND STORED VALUE OF OUTPUT SIGNAL AT TIME T_jIS LOST
208
LOW POWER MODE CONTROLLER SWITCHES FROM STANDBY MODE BACK TO OPERATIONAL MODE
210
IC INITIALISED SUCH THAT VALUE STORED BY DELAYED LATCH PASSED AS INPUT VALUE TO STAGE j+1
212

Fig 13

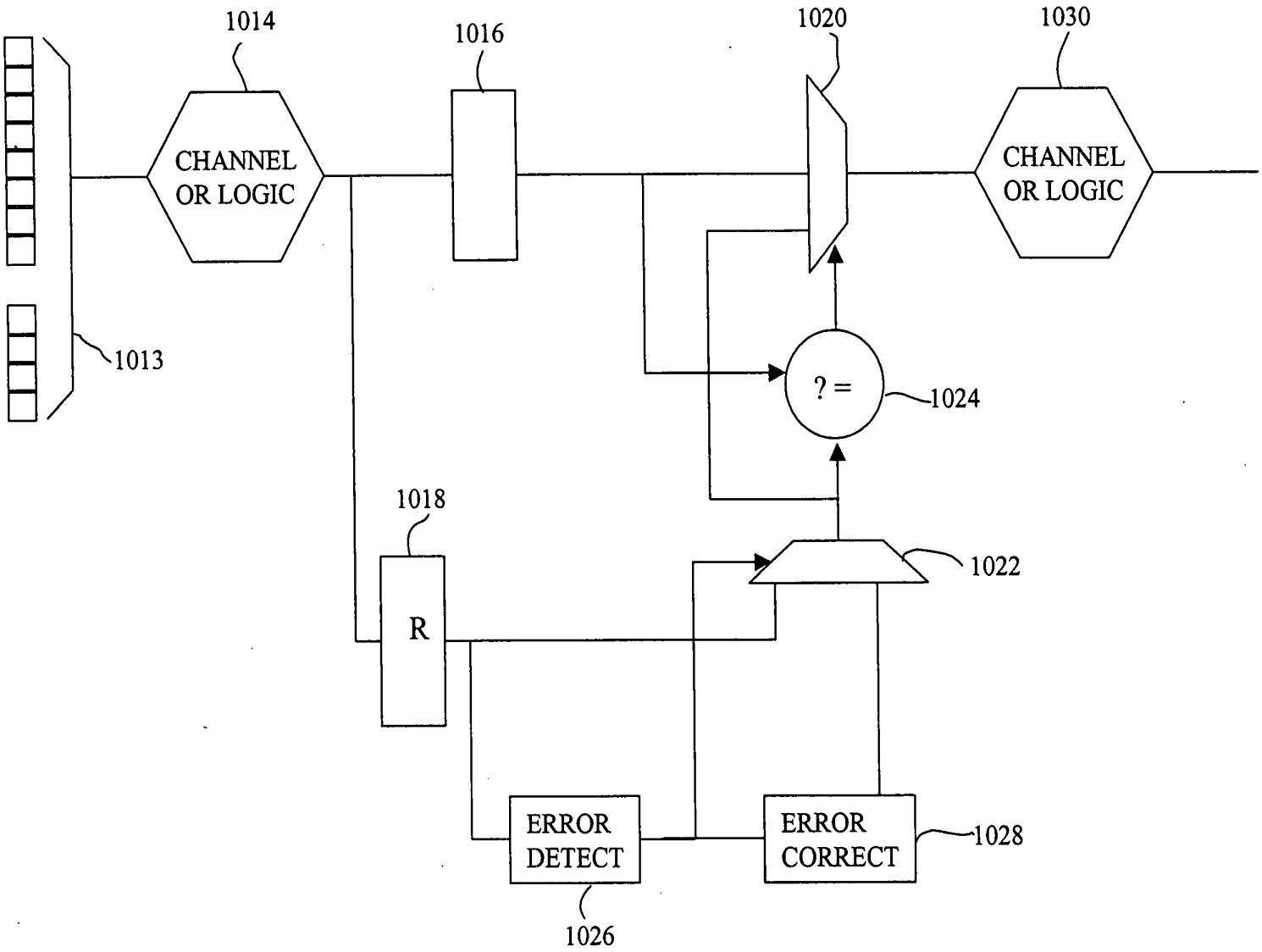

1014
1016
1020
1030
CHANNEL OR LOGIC
CHANNEL OR LOGIC
1013
? =
1024
1018
1022
R
ERROR DETECT
ERROR CORRECT
1028
1026

Fig 14

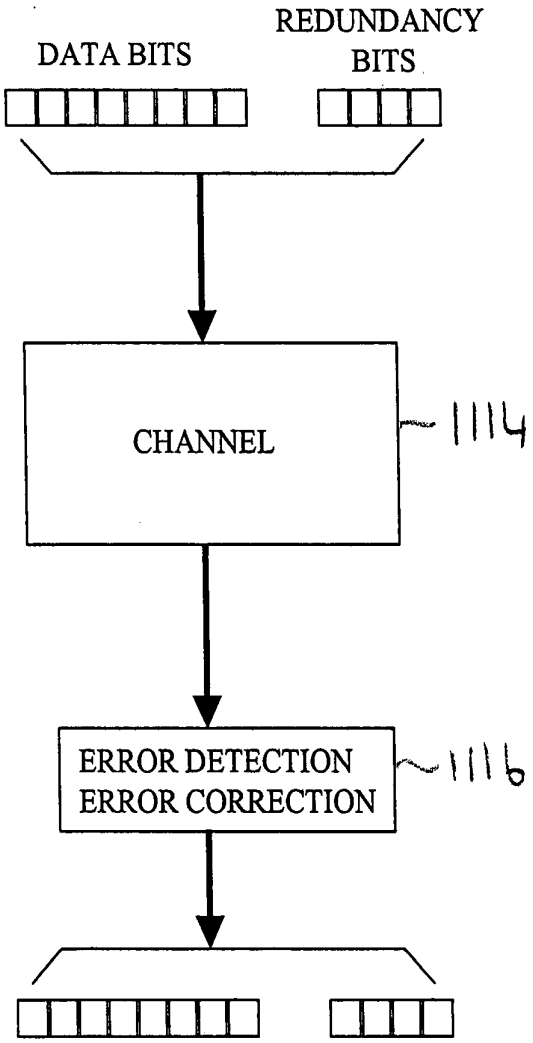

DATA BITS
REDUNDANCY BITS
CHANNEL
1114
ERROR DETECTION
ERROR CORRECTION
1116

Fig 15

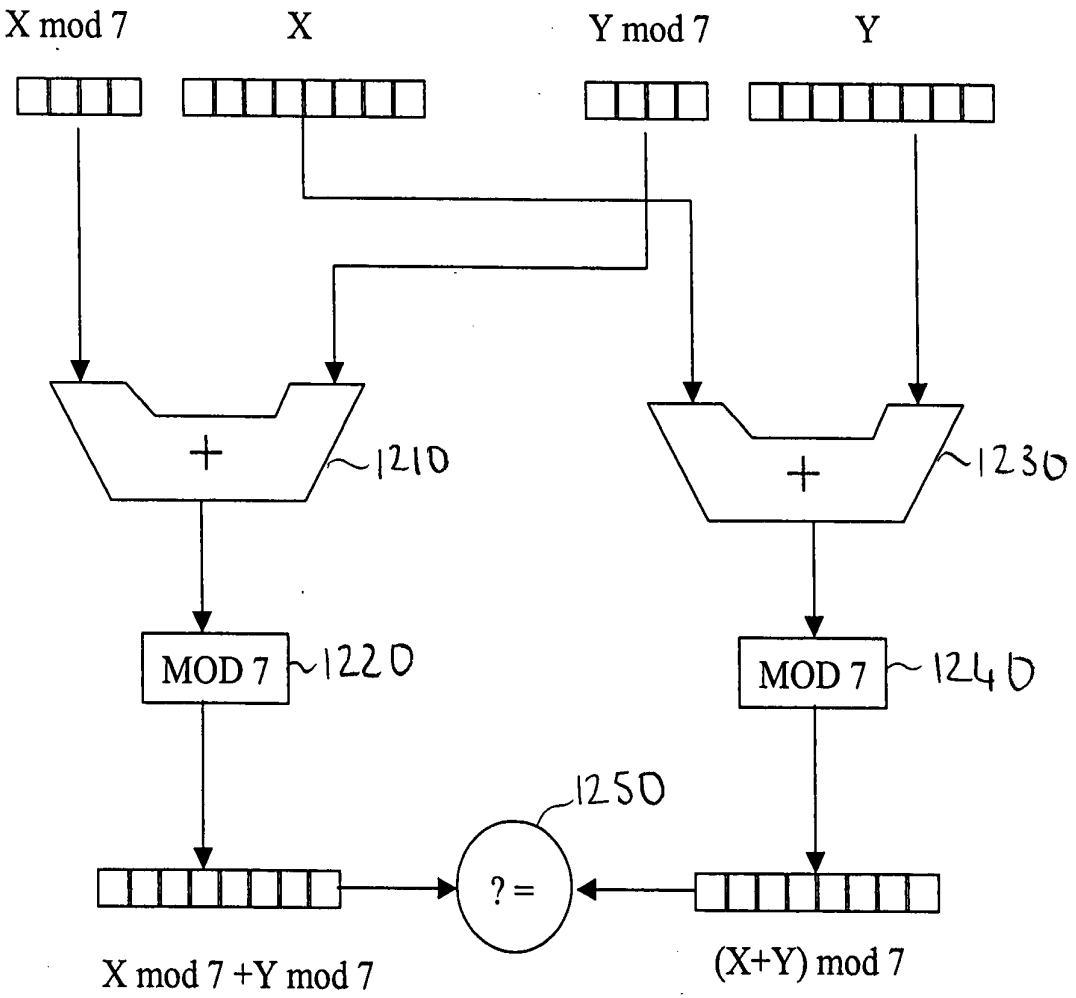

X mod 7
X
Y mod 7
Y
+
1210
+
1230
MOD 7
1220
MOD 7
1240
1250
?=
X mod 7 +Y mod 7
(X+Y) mod 7

Fig 16

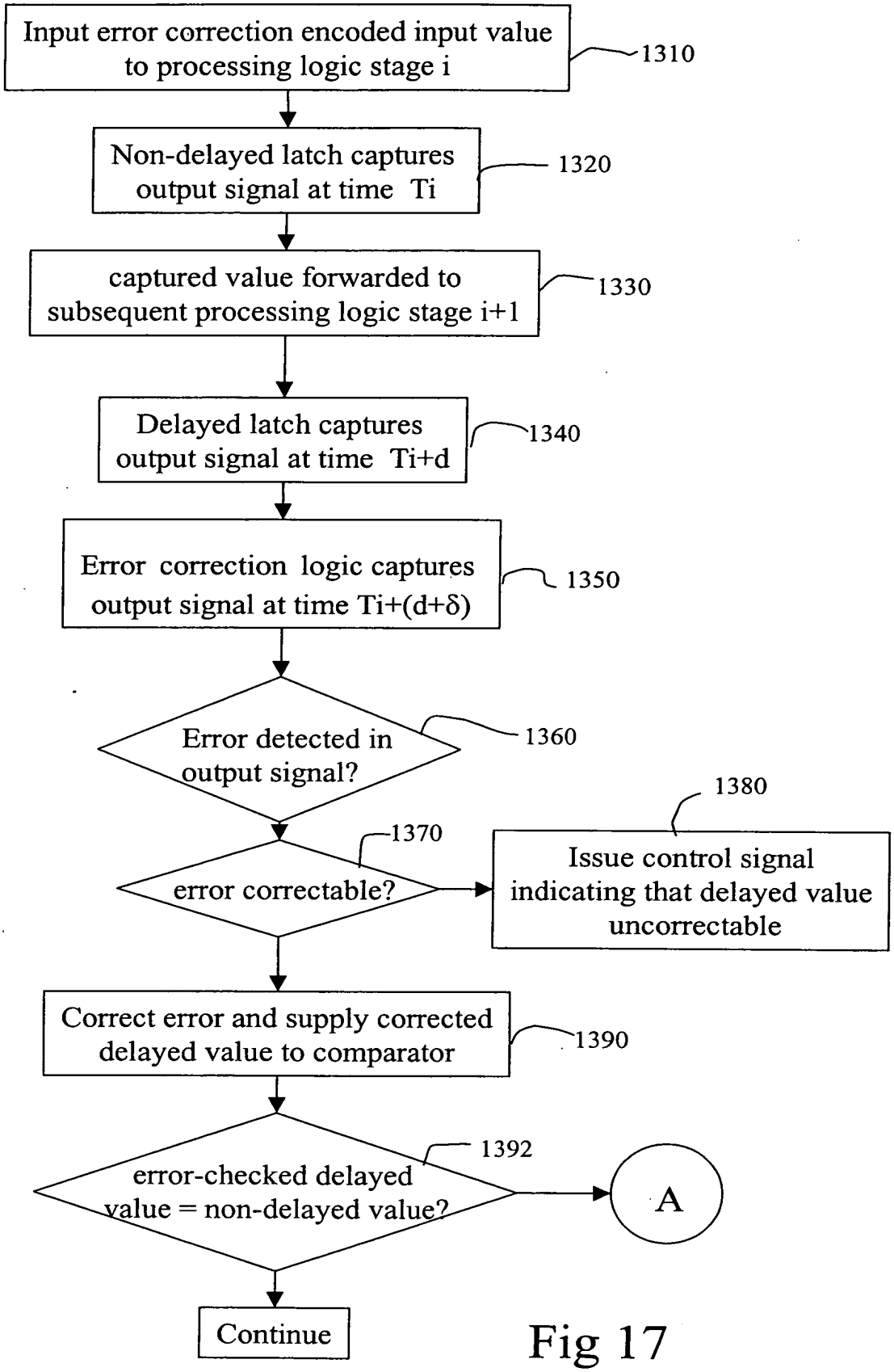

Input error correction encoded input value to processing logic stage i
1310
Non-delayed latch captures output signal at time Ti
1320
captured value forwarded to subsequent processing logic stage i+1
1330
Delayed latch captures output signal at time Ti+d
1340
Error correction logic captures output signal at time Ti+(d+δ)
1350
Error detected in output signal?
1360
1380
1370
error correctable?
Issue control signal indicating that delayed value uncorrectable
Correct error and supply corrected delayed value to comparator
1390
1392
error-checked delayed value = non-delayed value?
A
Continue

Fig 17

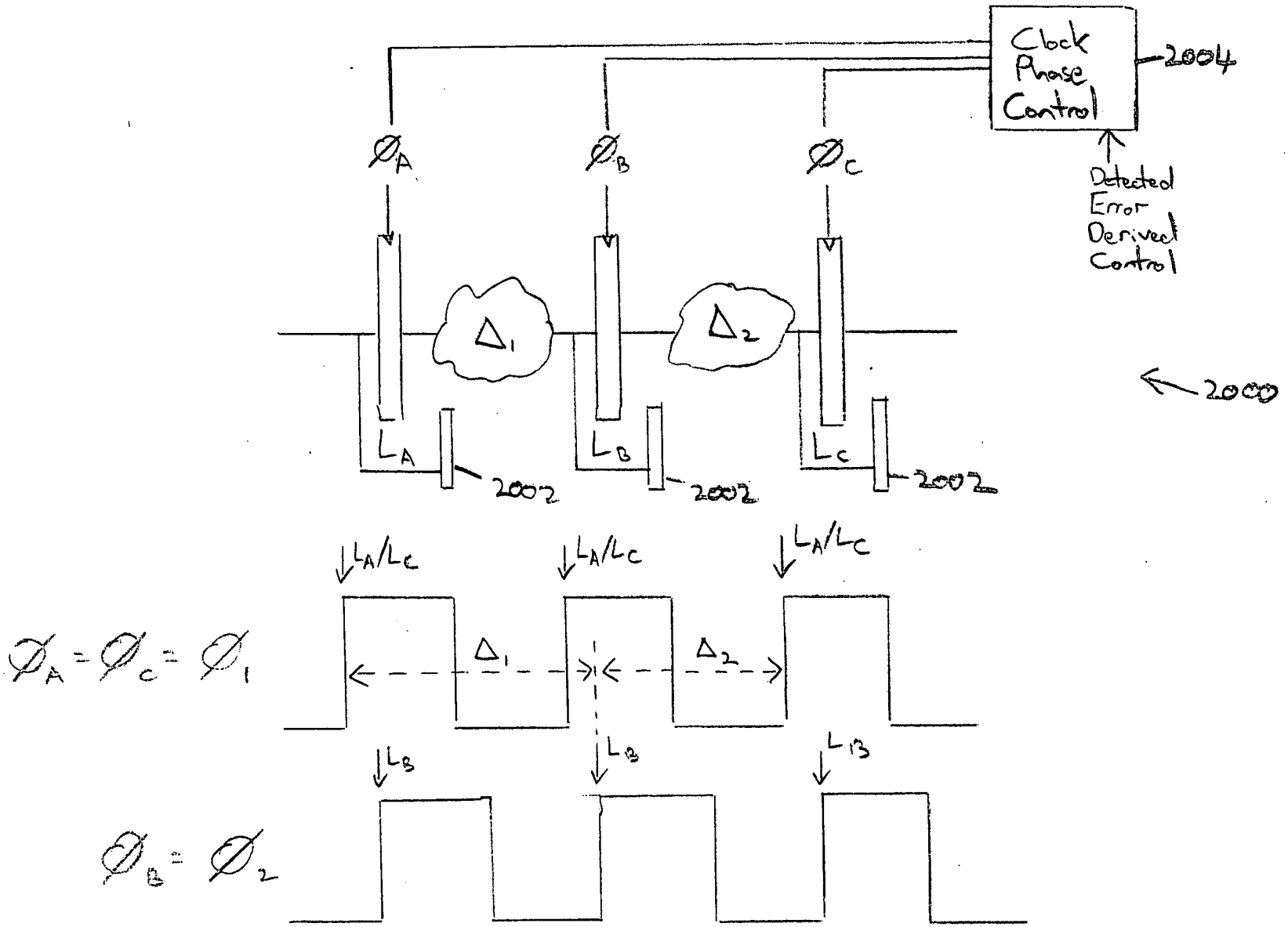
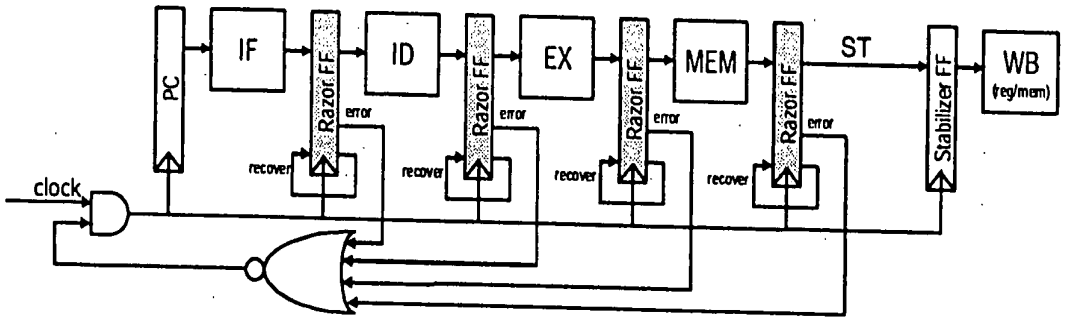

Clock Phase Control
2004
Detected Error Derived Control
ϕ_A
ϕ_B
ϕ_C
Δ_1
Δ_2
L_A
L_B
L_C
2002
2002
2002
2000
L_A/L_C
L_A/L_C
L_A/L_C
$\phi_A = \phi_C = \phi_1$
Δ_1
Δ_2
L_B
L_B
L_B
$\phi_B = \phi_2$

Fig 18


PC
IF
Razor FF
ID
Razor FF
EX
Razor FF
MEM
Razor FF
ST
Stabilizer FF
WB
(reg/mem)
error
recover
clock

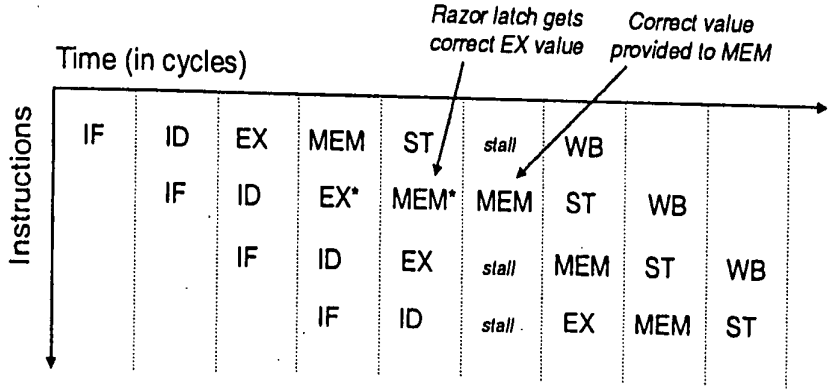
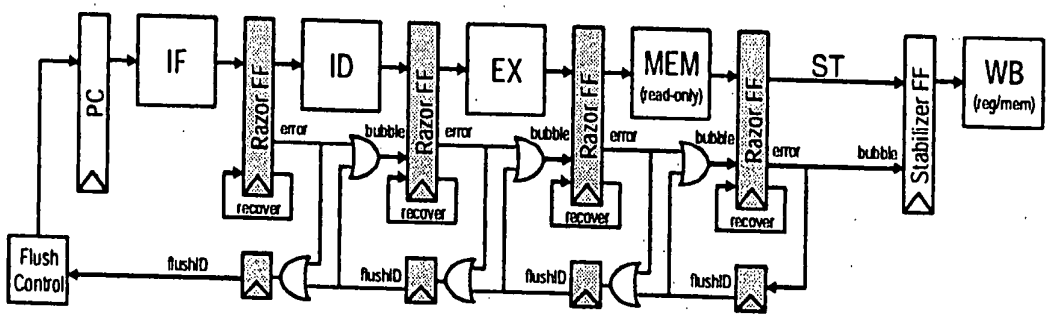

Razor latch gets correct EX value
Correct value provided to MEM
Time (in cycles)
Instructions
IF ID EX MEM ST stall WB
IF ID EX* MEM* MEM ST WB
IF ID EX stall MEM ST WB
IF ID stall EX MEM ST

Fig 19


PC
IF
Razor FF
ID
Razor FF
EX
Razor FF
MEM
(read-only)
Razor FF
ST
Stabilizer FF
WB
(reg/mem)
error
bubble
recover
Flush
Control
flushID

a)

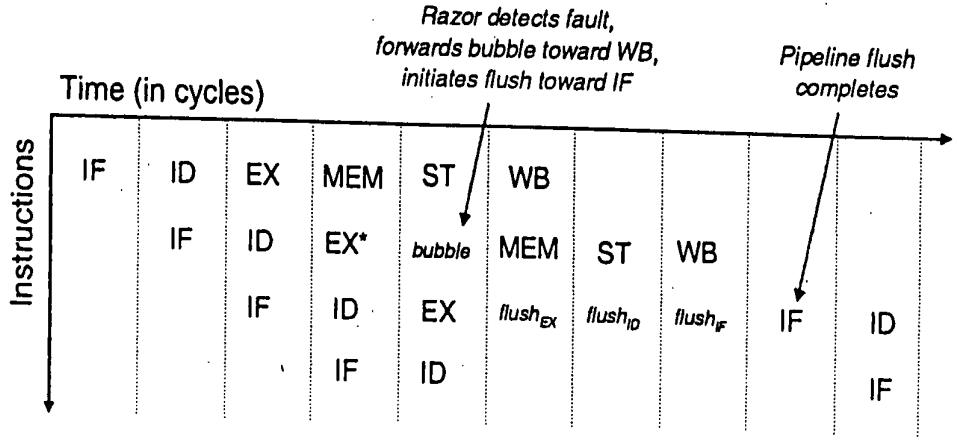

Razor detects fault,
forwards bubble toward WB,
initiates flush toward IF
Pipeline flush
completes
Time (in cycles)
Instructions
IF
ID
EX
MEM
ST
WB
bubble
flush_EX
flush_ID
flush_IF

Fig 2c

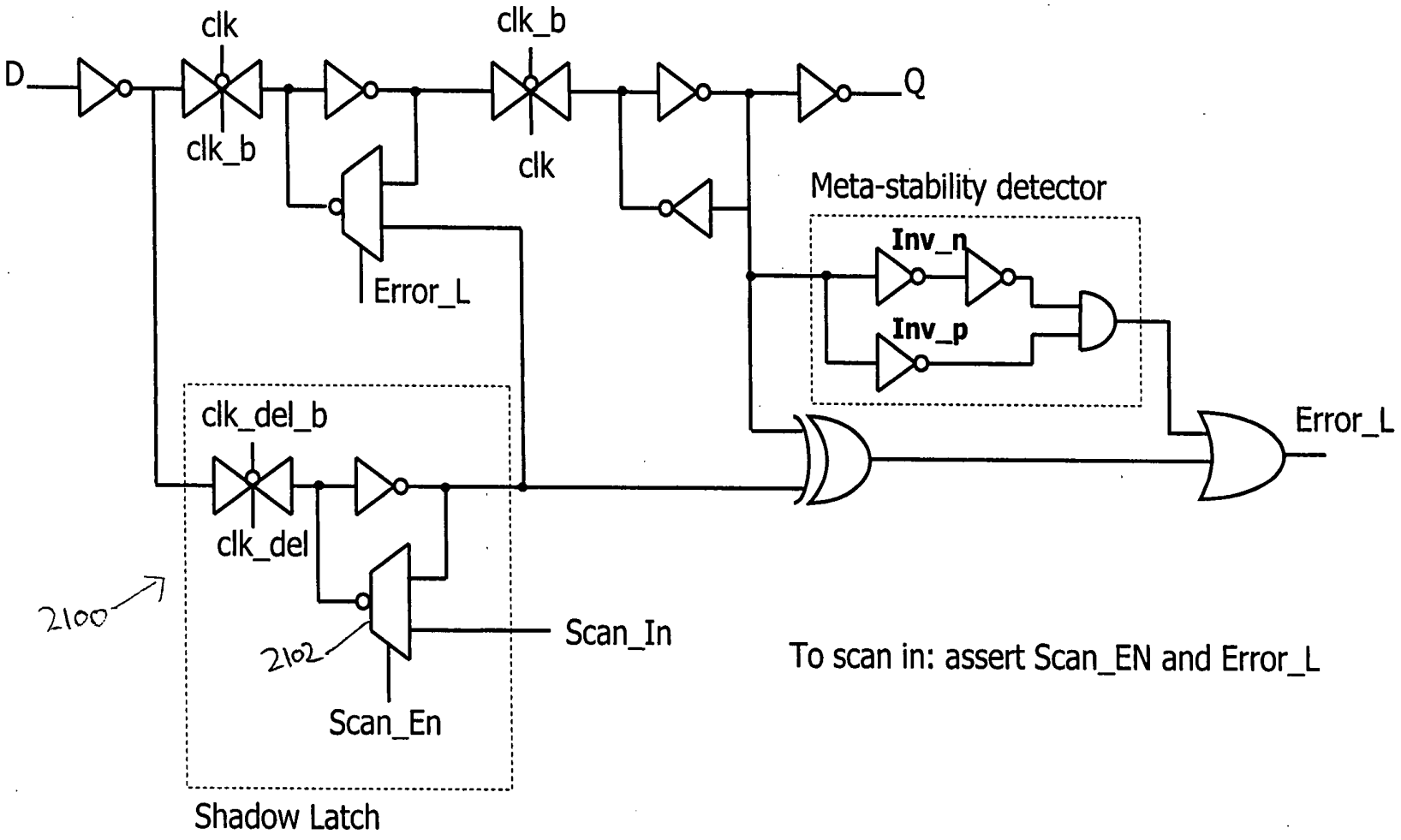

D
clk
clk_b
clk_b
clk
Q
Error_L
Meta-stability detector
Inv_n
Inv_p
Error_L
clk_del_b
clk_del
2100
2102
Scan_In
Scan_En
Shadow Latch
To scan in: assert Scan_EN and Error_L

Fig. 21